MX·COM, INC.

MX406*

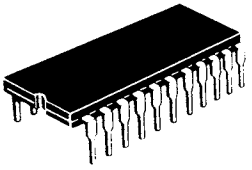
PHASE LOCKED FILTER

FEATURES:

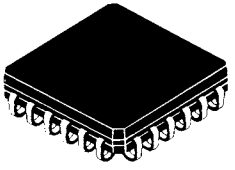
- 2nd Order Multiple Filter
- PLL Clock Generator
- Programmable Q
- F_c set by RC or External Clock
- Gain Adjustment on Inputs
- Low power CMOS Requirement

APPLICATIONS:

- Programmable Filters
- Voltage Controlled Filters
- Sinewave Oscillators
- Tracking Filters/Oscillators
- FSK and PSK Modems
- Square-Sine, Pulse-Sine Converters



MX406J (CDIP)
MX406P (PDIP)
22 pins



MX406LH
(24p PLCC)

DESCRIPTION:

The MX406 is a CMOS LSI circuit with a wide variety of signal processing applications. As depicted in Figure 1, the device consists of a 2nd order switched capacitor filter with a single input and separate bandpass, notch, lowpass, and highpass outputs. An on-chip clock generator provides the switched capacitor sampling clock frequency.

The center frequencies of the bandpass and notch filters are the same as the cut-off frequency f_c of the lowpass and highpass filters. The filter sampling clock is derived from a multiplying phase locked loop whose reference frequency is identical to the desired filter cut-off frequency.

The PLL is comprised of a voltage controlled oscillator, one of two types of phase comparator, a fixed divider, and an external RC loop filter. The filter cut-off frequency may be programmed by injecting an external signal into the PLL, or by using the on-chip oscillator circuit. The filters have input gain adjustment and the Q is programmable to eight values between 0.54 and 8.0.

*Application notes are included in Section 3 of this catalog.

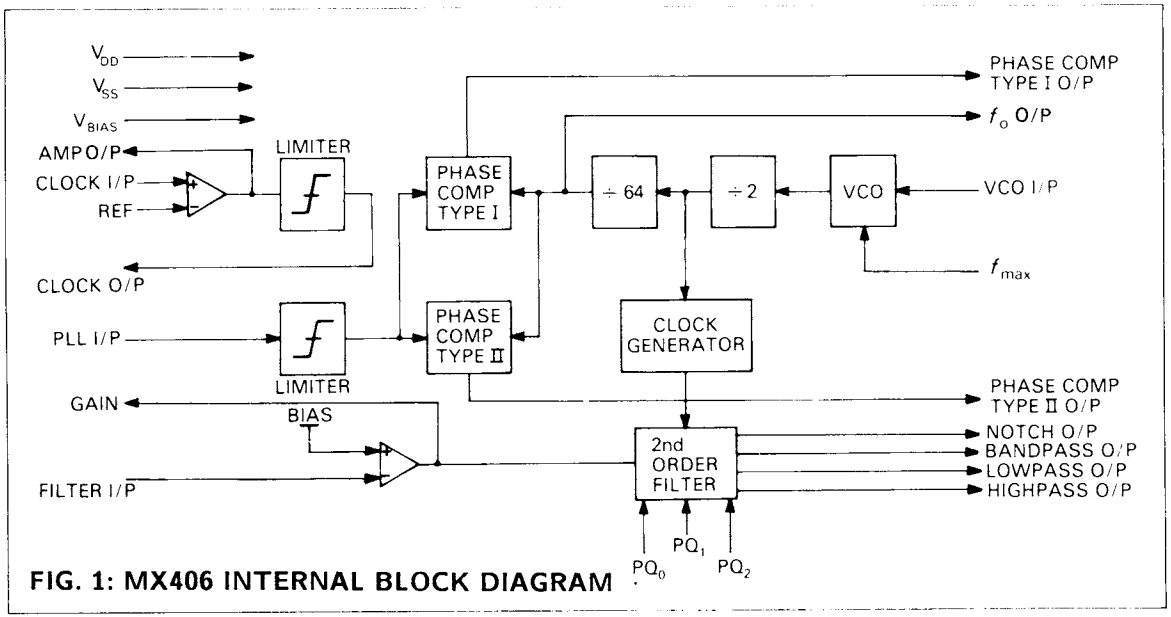


FIG. 1: MX406 INTERNAL BLOCK DIAGRAM

MX406 PIN FUNCTION TABLE

PIN		FUNCTION/DESCRIPTION
MX406J MX406P	**MX406LH**	
1	1	**PCI O/P:** Output of 'EXCLUSIVE-OR' type phase comparator. See Note on PLL operation.
2	2	**PLL I/P:** Input to limiter preceding phase comparators.
3	4	**f_o O/P:** Divided down VCO square wave output.
4	5	**PQ_0:**
5	6	**PQ_1:** } **I/P:** These pins set the Q of the filters; they have internal resistors to set Q = 0.71 if left open circuit. Possible Q values are:
6	7	**PQ_2:**

PQ_0	PQ_1	PQ_2	Q
1	1	1	0.54*
0	1	1	0.58 (Bessell)
1	0	1	0.71 (Butterworth)
0	0	1	1.00
1	1	0	1.31
0	1	0	2.00
1	0	0	4.00
0	0	0	8.00

*(Cascaded with a 1.31 section for a 4th order Butterworth filter).

7	8	**Clock O/P:** Digital output of clock oscillator circuit.
8	10	**Amp O/P:** Analog output of clock oscillator amplifier.
9	11	**Reference:** Inverting input to clock oscillator amplifier.
10	12	**Clock I/P:** Non-inverting input to clock oscillator amplifier.
11	13	**VSS:** Negative supply.
12	14	**V_{bias}:** VDD/2 bias pin, externally decoupled.
13	15	**Filter I/P:** Input to filter input buffer amplifier.
14	16	**Gain:** Output of filter input buffer amplifier.
15	17	**Highpass O/P:** Output of the highpass filter. The cut-off frequency is identical to the input frequency to the PLL when locked.
16	18	**Lowpass O/P:** Output of the lowpass filter. The cut-off frequency is the same as the highpass filter.
17	19	**Bandpass O/P:** Output of the bandpass filter. f_o is identical to the input frequency to the PLL when locked. Gain in passband is dependent on Q.
18	20	**Notch O/P:** Output of the notch filter, f_o, is the same as the bandpass filter.
19	21	**VCO I/P:** Input of the VCO control voltage, usually connected to loop filter output.

MX406 PIN FUNCTION TABLE

PIN		FUNCTION/DESCRIPTION
MX406J MX406P	**MX406LH**	
20	**22**	**f_{MAX}:** This pin is connected to VSS via an external resistor. The value sets the maximum frequency of operation of the VCO.
21	**23**	**PCII O/P:** Output of the edge-triggered type of phase comparator. See note on PLL operation.
22	**24**	**VDD:** Positive supply.
-	**3,9**	**No Connection:** Leave open-circuit.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (Total)	20mA
Maximum Device Dissipation	100mW
Operating Temperature	-30°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=5.0V

T_{AMB}=25°C

PLL input = 1kHz

Filter Q = 0.707

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current		-	4.5	8.5	mA
Input Impedance					
Filter & Clock Osc.		1.0	-	-	MΩ
PQ0, PQ1, PQ2		250	-	-	kΩ
Output Impedance					
Filter Outputs		-	-	1.0	kΩ
Clock Outputs		-	-	1.0	kΩ
Input logic 1		70% V_{DD}	-	-	V
Input logic 0		-	-	30% V_{DD}	V

Characteristics	See Note	Min.	Typ.	Max.	Unit
Filter Characteristics					
Maximum Cutoff Frequency		4.0	5.0	-	kHz
Minimum Cutoff Frequency		-	50	100	Hz
Gain at f_c (f_0) (HP BP LP)		-	20 log Q	-	dB
Notch Filter Depth	1	-	-30	-	dB
Notch Accuracy	1	-	±0.5% f_0	-	Hz
Maximum Signal Handling	2	3.0	-	-	V p-p
No signal filter noise					
BP		-	6.0	-	mVrms
LP HP N		-	3.0	-	mVrms
VCO Characteristics					
VCO* Maximum Frequency	3	4.0	5.0	-	kHz
VCO* Minimum Frequency	3	-	50	100	Hz
Voltage to Frequency Linearity		-	±20	-	%
VCO Conversion Gain		-	100	-	kHz/V
VCO Input Impedance		1.0	-	-	MΩ
Phase Comparator Characteristics					
Input Impedance		100	500	-	kΩ
Input Sensitivity	4	30	10	-	mVrms
Output Impedance					
Edge Triggered	5	-	-	1.5	kΩ
XOR		-	-	1.5	kΩ
Amplifier Characteristics					
(Clock oscillator and Filter inputs)					
Open Loop Gain		40	-	-	dB
Input Offset Voltage		-	-	10	mV
Maximum Signal Handling	2	3.0	-	-	V p-p

NOTES:

1. Q = 8.

2. For SINAD = 30dB at output.

3. VCO Frequency divided down at f_0 output.

4. At PLL input pin, a.c. coupled.

5. Output impedance when conducting, output is high impedance three-state when PLL is in lock.

Typical Filter Frequency Responses

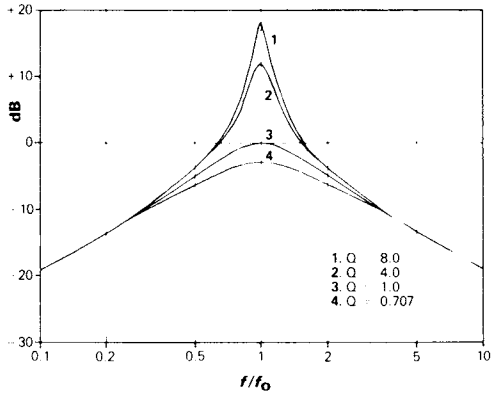


Fig. 2 Bandpass Frequency Response for different Q Values

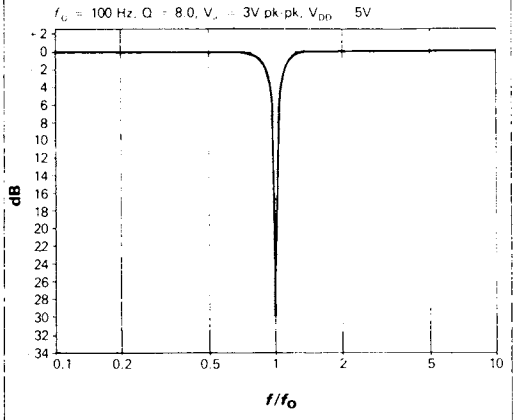


Fig. 3 Notch Frequency Response

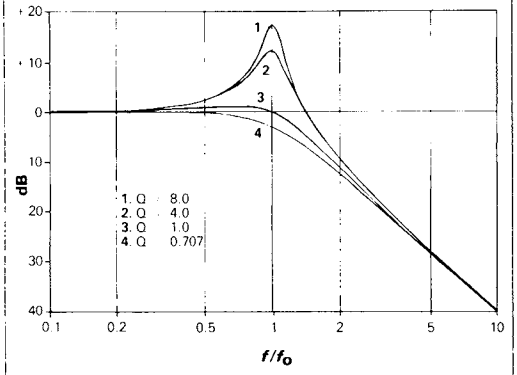


Fig. 4 Lowpass Frequency Response for different Q Values

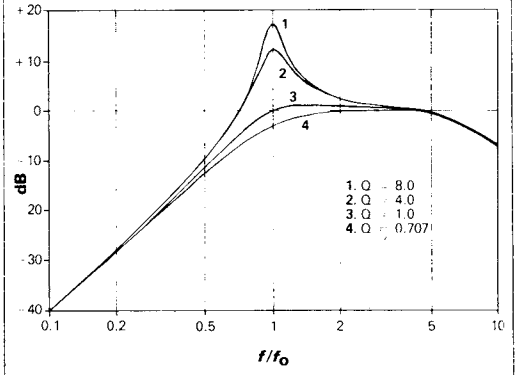


Fig. 5 Highpass Frequency Response for different Q Values

PC4060 PCB FOR DESIGN EVALUATION

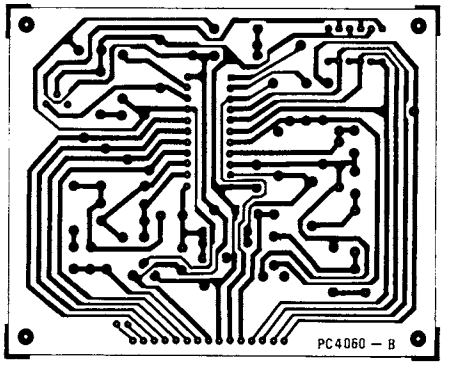


Fig. 6 (a) Track Side

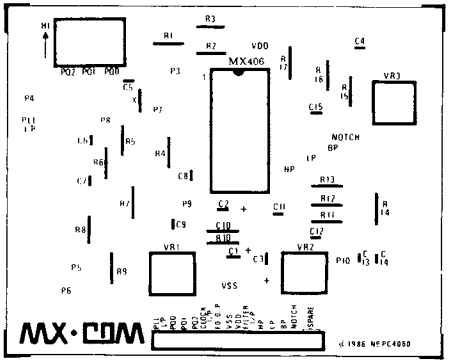


Fig. 6 (b) Component Side

Fig. 6 PC4060 Printed Circuit Board

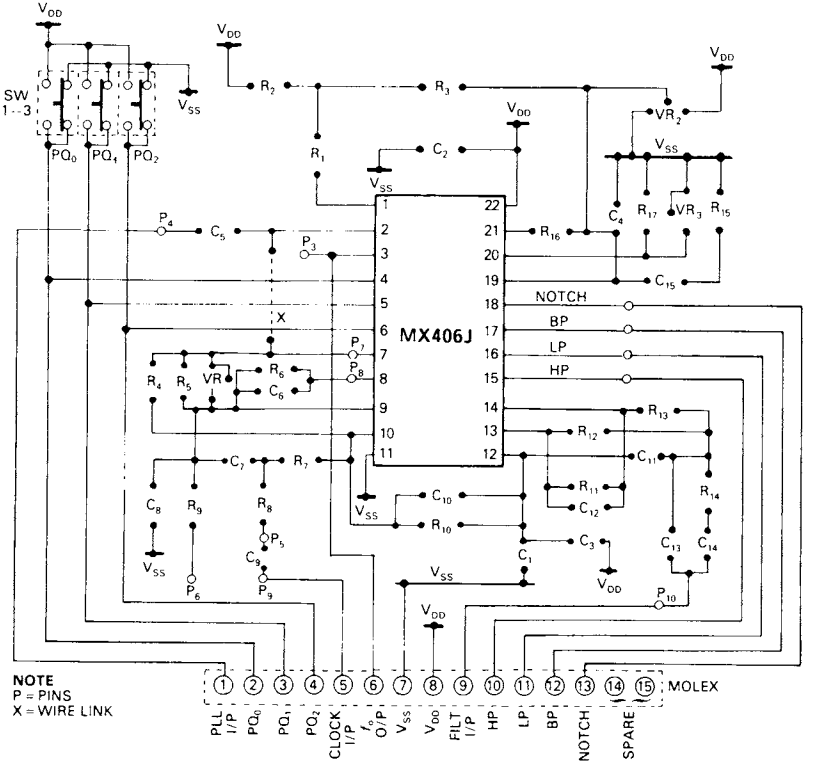


Fig. 6 (c) PC4060 Printed Circuit Board Schematic Diagram

External Component Connections

Two examples of MX406 external component connections are illustrated below. Component references are identical to PC4060 PCB circuit references.

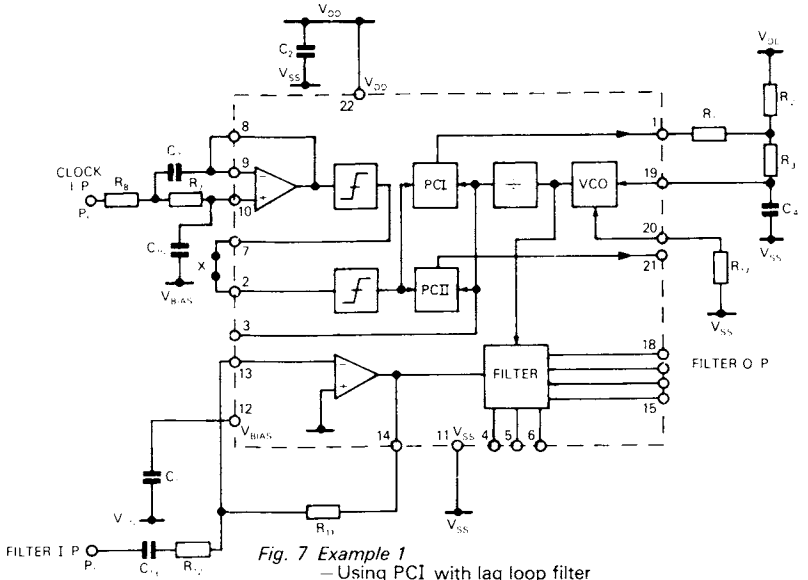


Fig. 7 Example 1

- Using PCI with lag loop filter
- VCO range set using R_{max} (R_{17}) and f_{min} potential divider (R_1, R_2)
- Filter input with simple gain adjustment
- Clock input pre-filtered with 2nd order LPF.

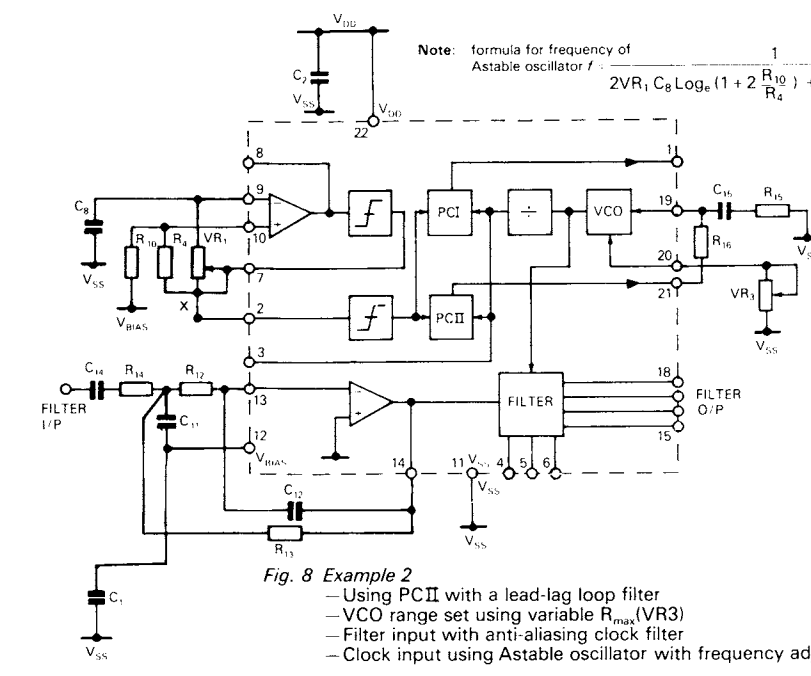


Fig. 8 Example 2

- Using PCII with a lead-lag loop filter
- VCO range set using variable R_{max}(VR3)
- Filter input with anti-aliasing clock filter
- Clock input using Astable oscillator with frequency adjustment